Printed Pages:01 **Sub Code: KEC-054**

Paper Id: | 2 | 3 | 1 | 9 | 9 | 8 | **Roll No.** | | | | | | | | | | | | |

B.TECH
(SEM V) THEORY EXAMINATION 2022-23
ADVANCE DIGITAL DESIGN USING VERILOG

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If you require any missing data, then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

(a) Describe the term mixed logic.
(b) Explain the Don't care (X) condition in digital design.
(c) Define the term comparator.
(d) What is a Boolean Function for any circuit or device?
(e) What is the term optimization digital design?
(f) Explain the term algorithms.
(g) What is defined as a fault?
(h) Describe the term factoring.
(i) Define the term sequential circuit.
(j) Describe the term Programmable logic family.

SECTION B

2. Attempt any *three* of the following: 10 x 3 = 30

(a) Explain different techniques used for Multiple output minimization.
(b) Design a 4:1 Multiplexer using minimum gates.
(c) Describe the mapping algorithm in detail with respect to digital design.
(d) Define different path sensitization methods in digital design.
(e) Explain with a block diagram the architecture of FPGA.

SECTION C

3. Attempt any *one* part of the following: 10 x 1 = 10

(a) Describe the XOR Pattern handling in digital design.
(b) Define the logic representation methods in mixed logic design.

4. Attempt any *one* part of the following: 10 x 1 = 10

(a) Describe the techniques and methods used in structural specifications logic circuits with Verilog.
(b) Design a 3:8 Decoder using minimum gates.

5. Attempt any *one* part of the following: 10 x 1 = 10

(a) Explain the working and applications of ASM charts in digital design.
(b) Define the working and applications of multi-level minimization and optimization in digital design.

6. Attempt any *one* part of the following: 10 x 1 = 10

(a) Explain the working and applications of BDD in digital design.
(b) Describe the techniques used to detect faults in digital circuits.

7. Attempt any *one* part of the following: 10 x 1 = 10

(a) Explain with a block diagram the architecture of ASIC.
(b) Elaborate with a block diagram the architecture of PLD.